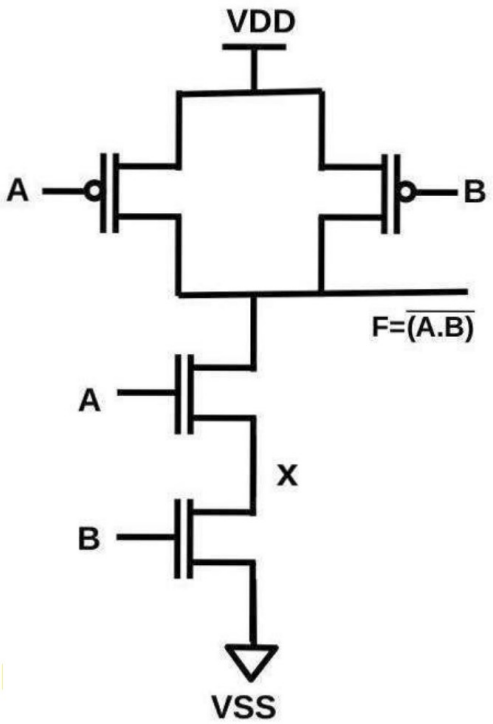
Static Timing Analysis (STA)

Henry Evans

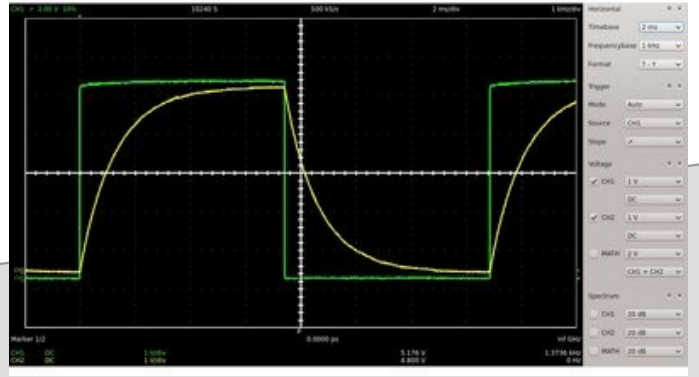
Who Am I

- Electrical Engineering Graduate, class of 2025
- Just moved to San Jose to start working at Astera Labs
- Enjoys hiking, camping, baking, and working on bikes

What Delays?

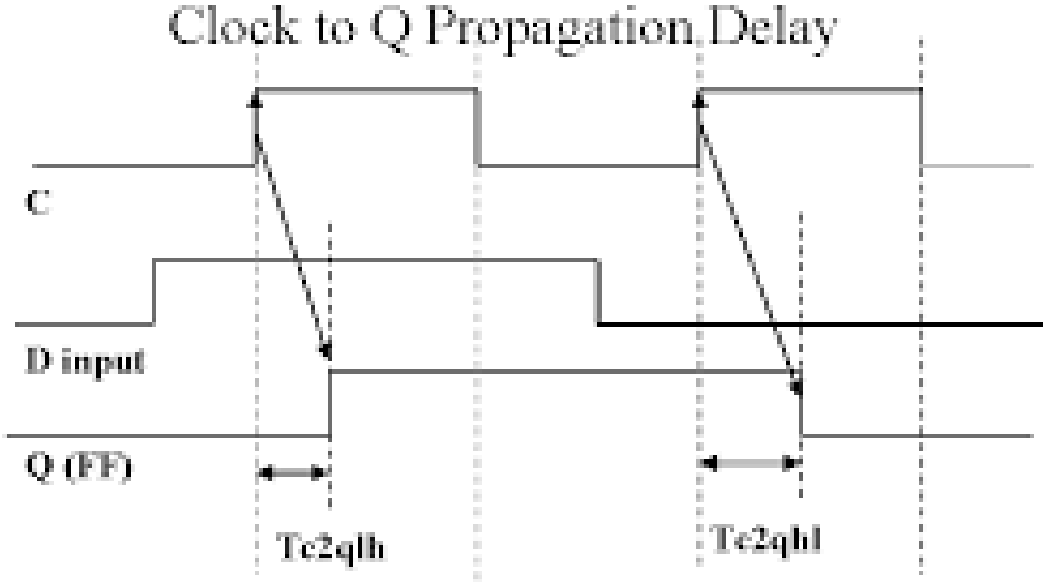


- Parasitic capacitance and resistance make transistors tiny RC circuits
- Long wires in the chip have LOTs of capacitance AND resistance
- Wires with larger fanouts have larger delays
- Gates with large fanins have larger delays



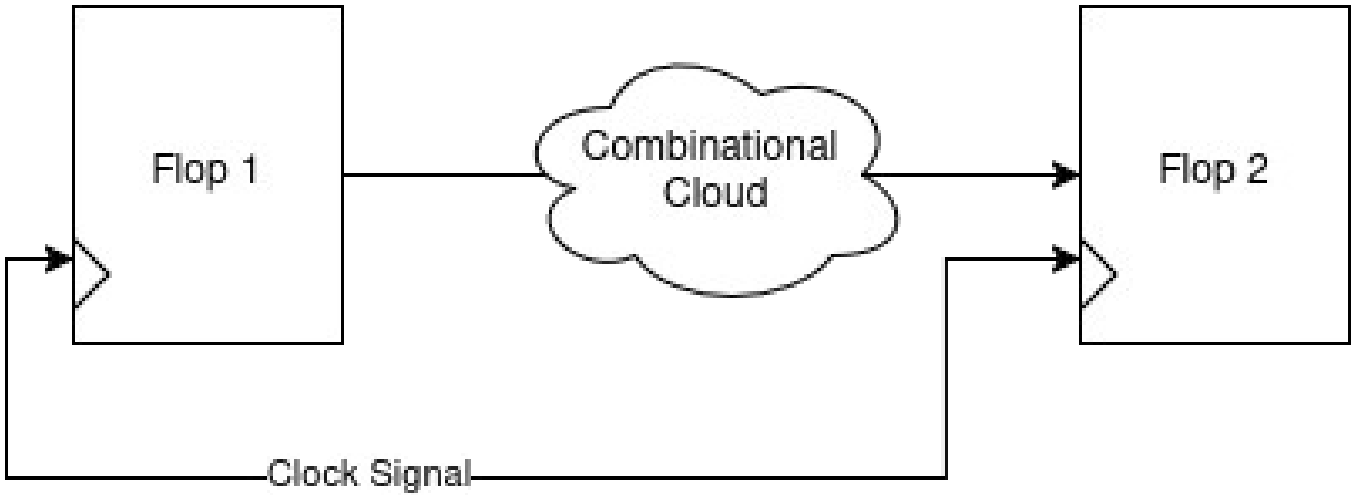
What Delays?

- Clock-Q delay



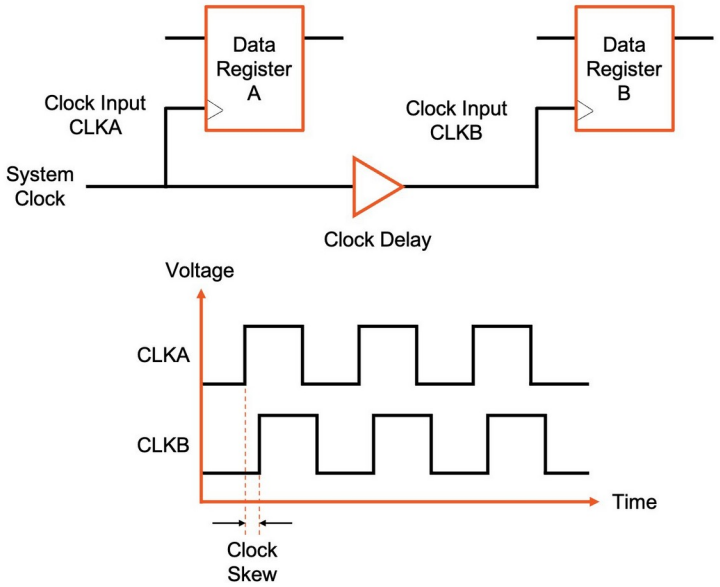
There is NO delay from D to Q!!! The clock input is what triggers the change, not the D input!!!

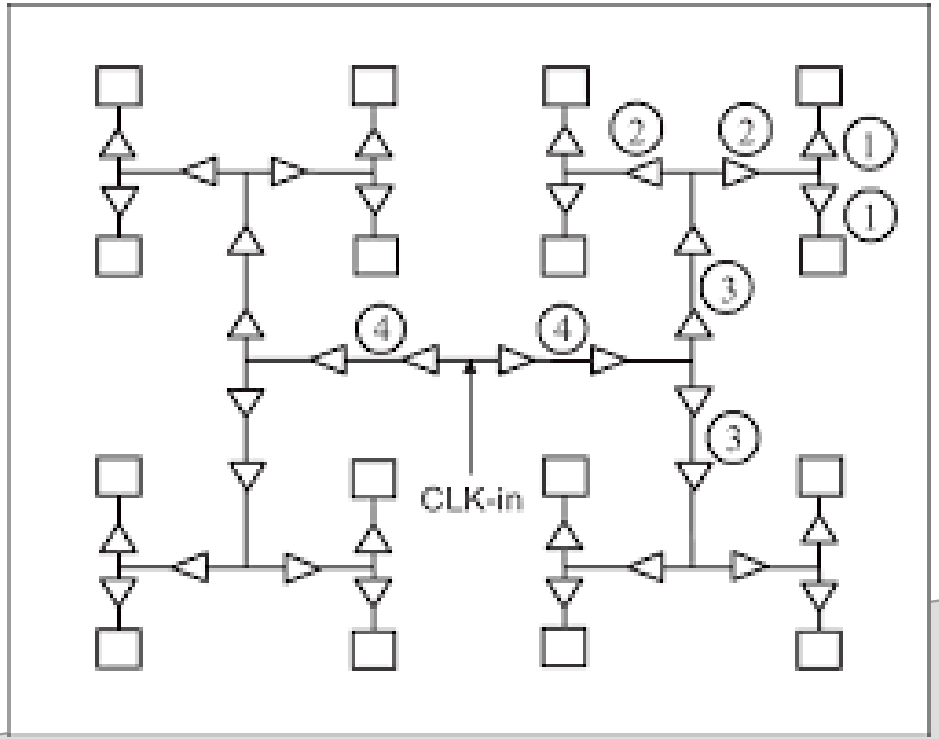
Who Cares?



Wait One More!

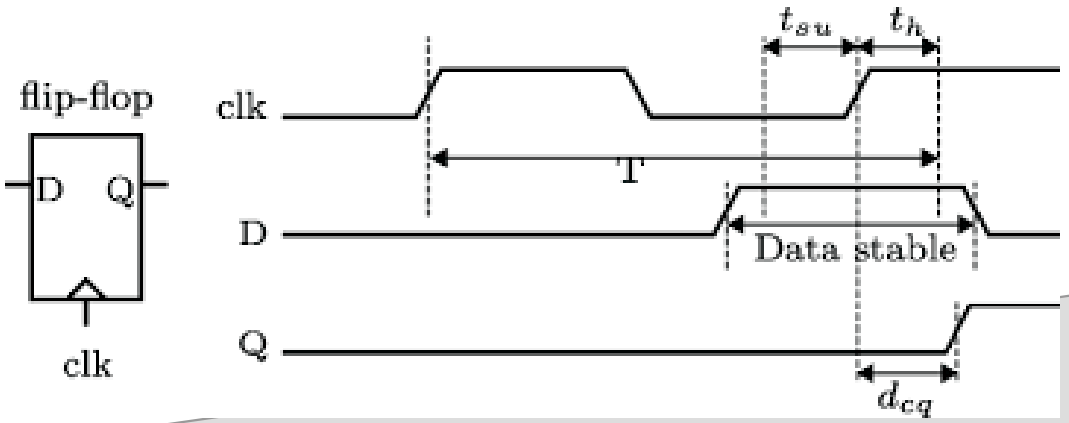
- Clock Skew!





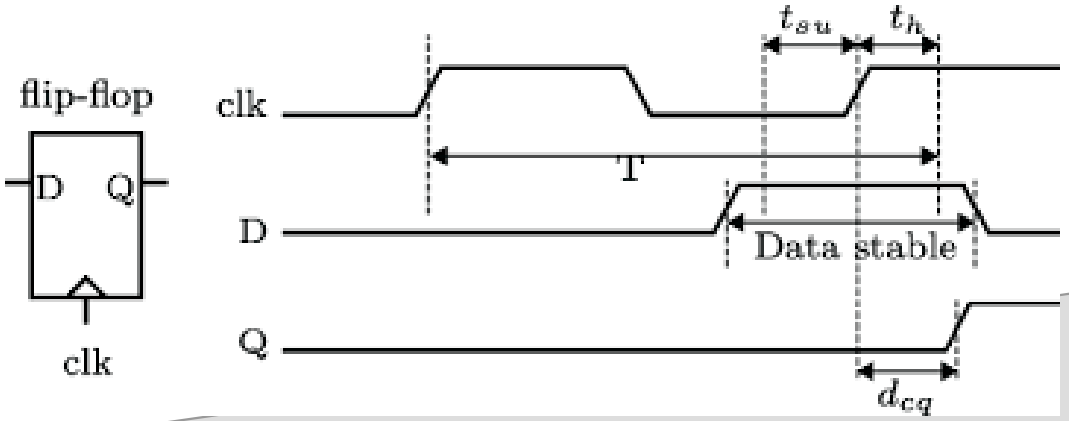
Setup Requirements

- All FF inputs must be stable *before* the rising clock edge
- This means we actually have *less* than one clock cycle to propagate our signals
- We can compensate by lowering the clock frequency



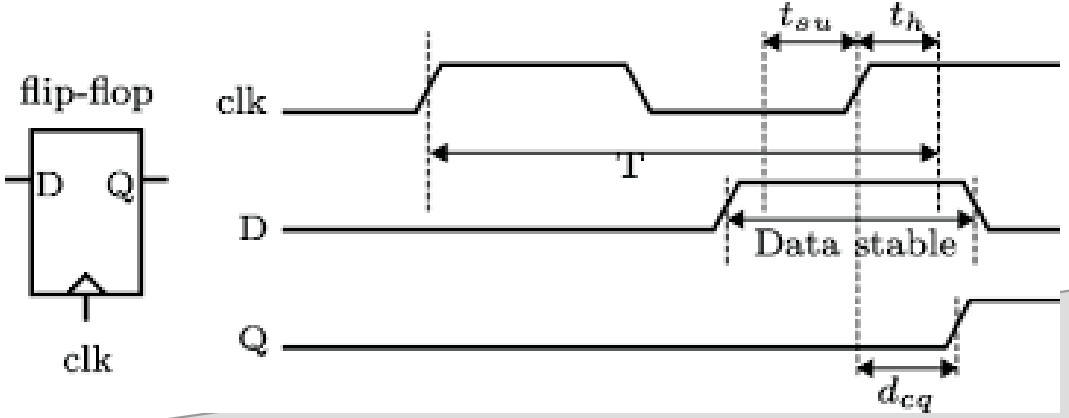
Hold Requirements

- All FF inputs *must* stay stable after the clock edge
- This create a minimum delay requirement on our signals
- Failing hold requirements can cause signals to “race” through multiple flops in a cycle
- Cannot be corrected post-tapeout



Metastability

- What happens if we violate setup/hold time requirements?
- Flip flops will sample a random in-between voltage
- This will eventually resolve to a 1 or 0, but we don't know which
- Really difficult to debug



Corners

- Becuase it isn’t hard enough…
- Signals propagate at different speeds based on:
  - Manufacturing variance
  - Operating temperature
  - Voltage
  - PMOS vs. NMOS variance

Corners

- PMOS vs. NMOS corners
  - Process variation can mean NMOS and PMOS devices have different characteristics
  - SS, FF, TT, FS, SF
  - SF and FS and the most concerning because the devices are behaving differently
- RC corners
  - Cworst, cbest, rcworst, rcbest
  - Largest/smallest capacitance/resistance in spec

STA In The Real World

- Seems really simple right?
- Much more complicated in the real world
  - input/output max delay constraints
  - Clock definitions (sync vs. async)
  - Clock crossings
  - Skew requirements
  - Case analysis
  - (sometimes) lots of scripting
- Will talk about this a bit more tomorrow

Questions?

Feel free to reach out!

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calcguy3.14 on Discord (in CPES & CARP)

Always happy to chat about tech, answer technical or non-technical questions