

Constraints 101

Henry Evans

What Are Constraints

- Tell the tool a little bit about your design
 - Clock definitions
 - Timing Exceptions
 - Input/Output Delay Requirements
 - Max Delay/Skew Requirements
 - Clock Groups
 - I/O definitions

IO Constraints

- Probably familiar with these from Basys3 board
- Define which I/O pins to map top level pins too
- The super weird names like W25 correspond to FPGA pin names

Clock Definitions

- Tell the tool where your clock generators are
 - PLLs, clock dividers, etc
- What frequency are your clocks?
- What duty cycle?
 - Only matters if using posedge and negedge

create_clock   

Create a clock object

Syntax

```
create_clock -period <arg> [-name <arg>] [-waveform <args>] [-add]
[-quiet]
[-verbose] [<objects>]
```



Clock Definitions

- `create_generated_clock` defines clocks generated from other clocks
- E.G. output of clock dividers
- Frequency is based on source clock

`create_generated_clock`

Create a generated clock object

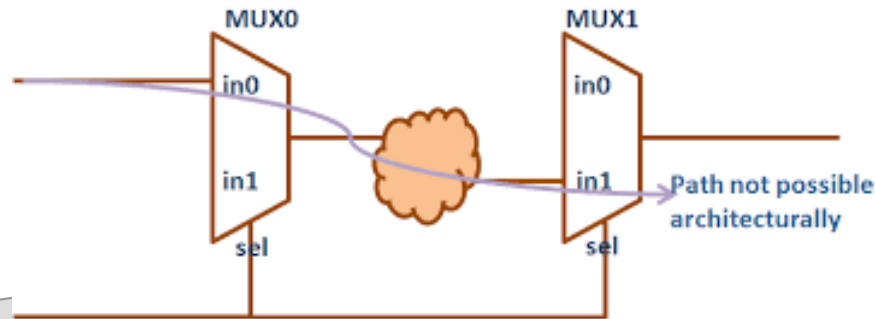
Syntax

```
create_generated_clock [-name <arg>] [-source <args>] [-edges <args>]  
    [-divide_by <arg>] [-multiply_by <arg>] [-combinational]  
    [-duty_cycle <arg>] [-invert] [-edge_shift <args>] [-add]  
    [-master_clock <args>] [-quiet] [-verbose] <objects>
```



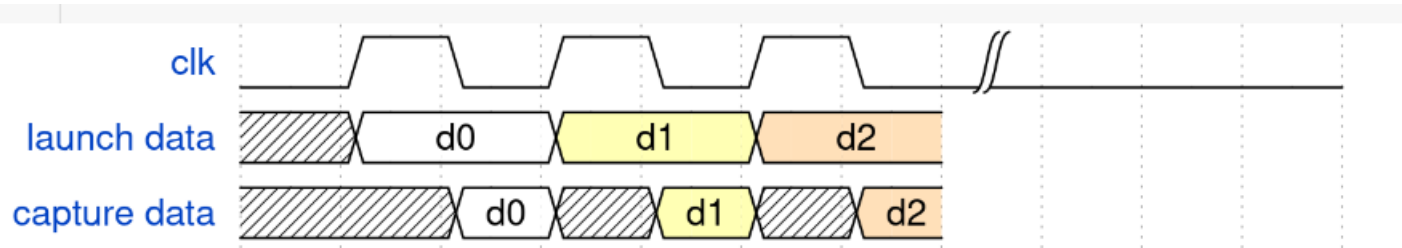
False Paths

- Sometimes the tool finds paths that will never be used in the actual design
- `set_false_path` tells the tool not to time or try to meet timing on a given path
- Only use if you're POSITIVE the path doesn't need to meet timing

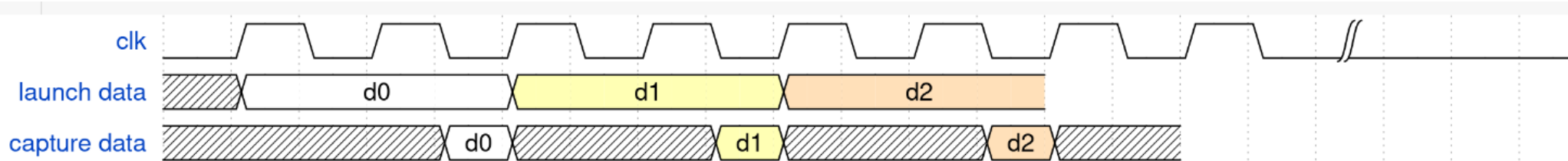
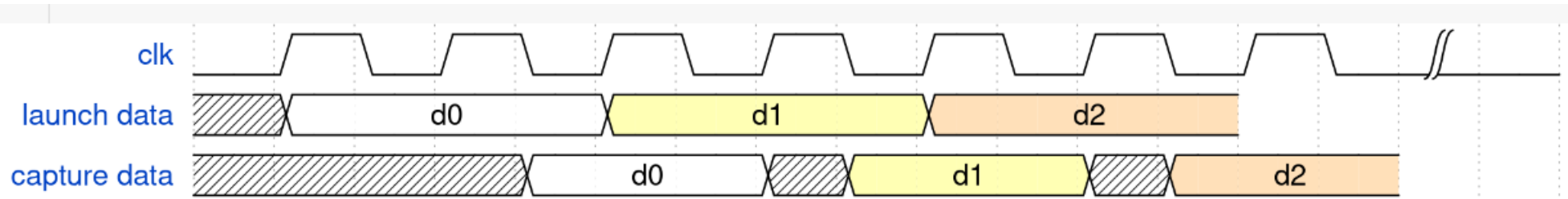
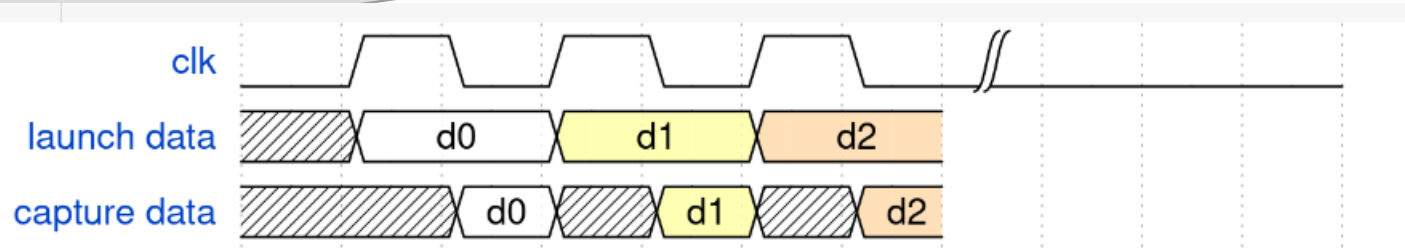


Multi Cycle Paths

- Allow a signal to take more than one cycle to get there
- CAUTION: many designers don't really know how these work



Multi Cycle Paths



Clock Groups

- Define the relationship between your clock signals
 - Synchronous?
 - Asynchronous?
 - Physically Exclusive?
 - Logically Exclusive?
- You have to be VERY sure before setting clocks as anything other than synchronous

All the Other Constraints...

- IO delay constraints – what delay is coming from outside the chip
- set_max_delay – tell the tool how much delay to tolerate irrespective of clocks
 - Useful for CDCs where there isn't a single clock to time to
- set_max_skew – how much difference in delay is acceptable between data signals
 - Also useful for CDCs and async FIFOs

Questions???

“

”