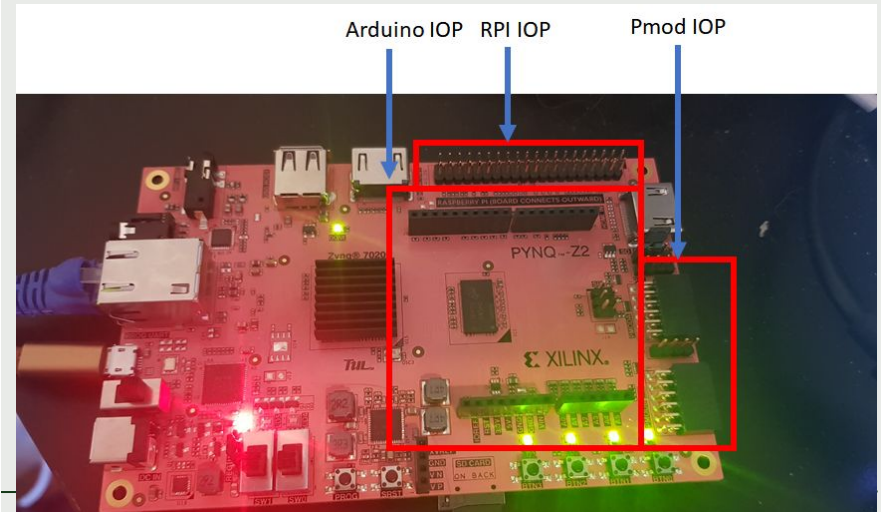
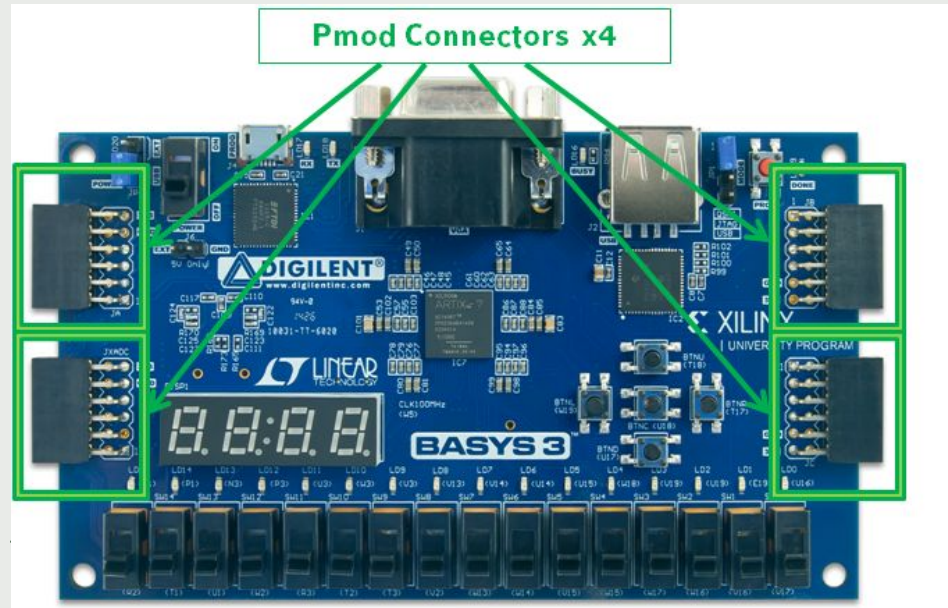
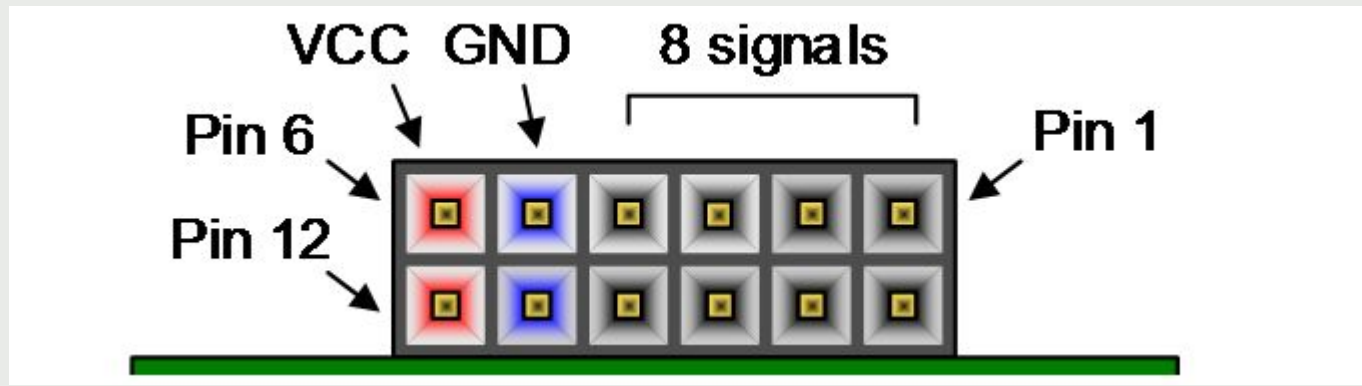


A quick word on PMOD

What is Pmod?

- **Pmod** stands for **Peripheral Module**.
 - It is a small hardware add-on interface commonly used with **FPGA boards**, microcontroller boards, and embedded systems.
 - Pmods let you quickly connect external hardware without designing a custom PCB.
 - **Examples of Pmod add-ons:**
 - Sensors
 - LCD/OLED displays
 - ADC/DAC boards
 - Bluetooth/Wi-Fi/GPS modules
 - SPI, UART, and I2C peripherals
 - **I will be using:**
 - GPIO Pmod
 - **I Plan to Use**
 - SPI Flash Memory Chip Pmod
 - SD Card Pmod
-

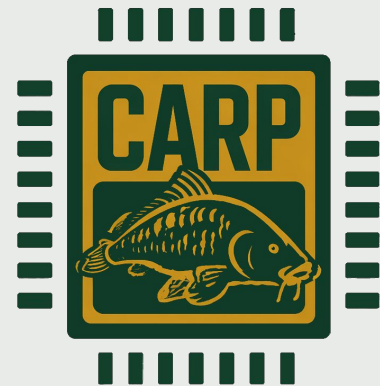


Just another option in the constraint file

It should already be in your
133 / 233 Constraint File.

```
124  ##Pmod Header JA
125  ##Sch name = JA1
126  set_property PACKAGE_PIN J1 [get_ports {P_LEDS[0]}]
127  set_property IOSTANDARD LVCMOS33 [get_ports {P_LEDS[0]}]
128  #Sch name = JA2
129  set_property PACKAGE_PIN L2 [get_ports {P_LEDS[1]}]
130  set_property IOSTANDARD LVCMOS33 [get_ports {P_LEDS[1]}]
131  #Sch name = JA3
132  set_property PACKAGE_PIN J2 [get_ports {P_LEDS[2]}]
133  set_property IOSTANDARD LVCMOS33 [get_ports {P_LEDS[2]}]
134  #Sch name = JA4
135  set_property PACKAGE_PIN G2 [get_ports {P_LEDS[3]}]
136  set_property IOSTANDARD LVCMOS33 [get_ports {P_LEDS[3]}]
137  ##Sch name = JA7
138  #set_property PACKAGE_PIN H1 [get_ports {JA[4]}]
139  #   set_property IOSTANDARD LVCMOS33 [get_ports {JA[4]}]
140  ##Sch name = JA8
141  #set_property PACKAGE_PIN K2 [get_ports {JA[5]}]
142  #   set_property IOSTANDARD LVCMOS33 [get_ports {JA[5]}]
143  ##Sch name = JA9
144  #set_property PACKAGE_PIN H2 [get_ports {JA[6]}]
145  #   set_property IOSTANDARD LVCMOS33 [get_ports {JA[6]}]
146  #Sch name = JA10
147  set_property PACKAGE_PIN G3 [get_ports MOTOR_PIN]
148  set_property IOSTANDARD LVCMOS33 [get_ports MOTOR_PIN]
149
```

Multiple Partitions. DFX



For DFX Basics, Ryan made an AMAZING, Literal, Step-by-step guide with a screenshots on every step here:

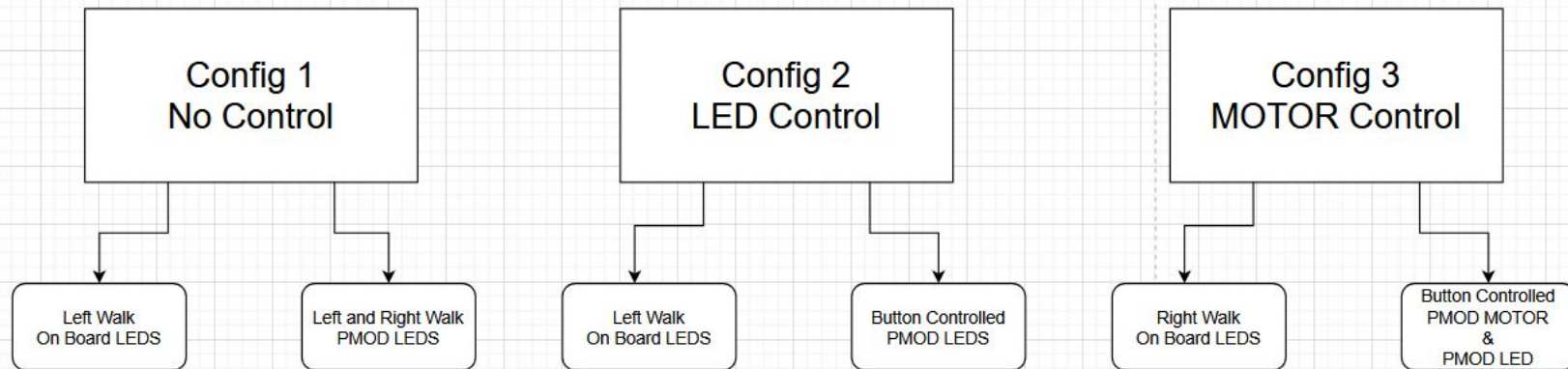
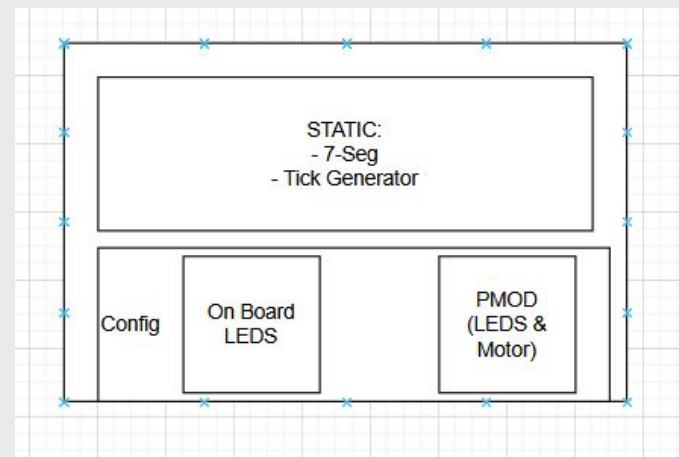
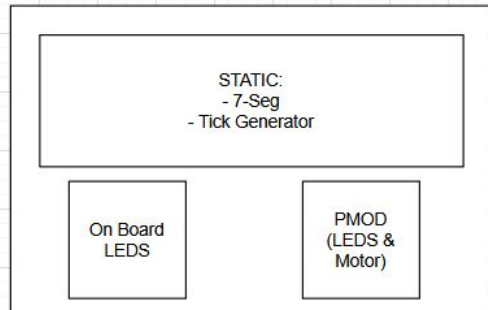
DFX tutorial for Block Design using the Basys 3

https://github.com/ryancramuh/fpga-embedded/tree/dfx-demos/dfx_w_RTL

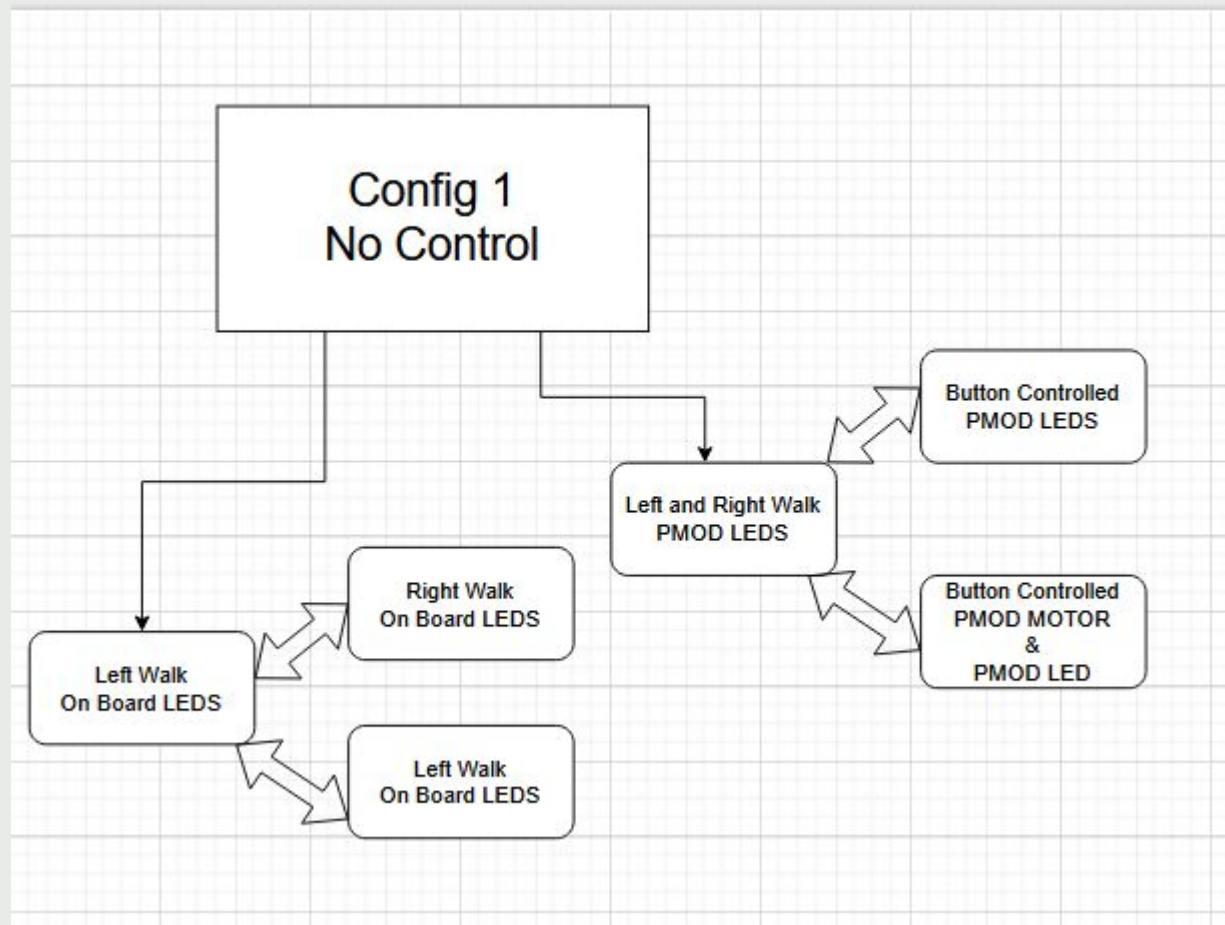
Having multiple Reconfigurable Blocks

Say you have P-Block A & P-Block B

1. Have your I/O control many things. Switch between what you're controlling/ inputting to by reconfiguring a block.
 2. You're only changing Block A while Block B AND the STATIC module keeps running.
 3. Have Pre-Set Configurations
-



The Partial BitStream Part



Make Sure all your Configs are the children of 1 Implementation

Reconfigurable Module Associations with Partition Definitions

Reconfigurable Module	Partition Definition
LED_LeftWalk	reconfig_OnBoardLEDS
LED_rightWalk	reconfig_OnBoardLEDS
PMOD_LeftRight	reconfig_PMOD
PMOD_LightControl	reconfig_PMOD
PMOD_MotorCNTRL	reconfig_PMOD
PMOD_MotorON	reconfig_PMOD
PMOD_MotorPULSE	reconfig_PMOD

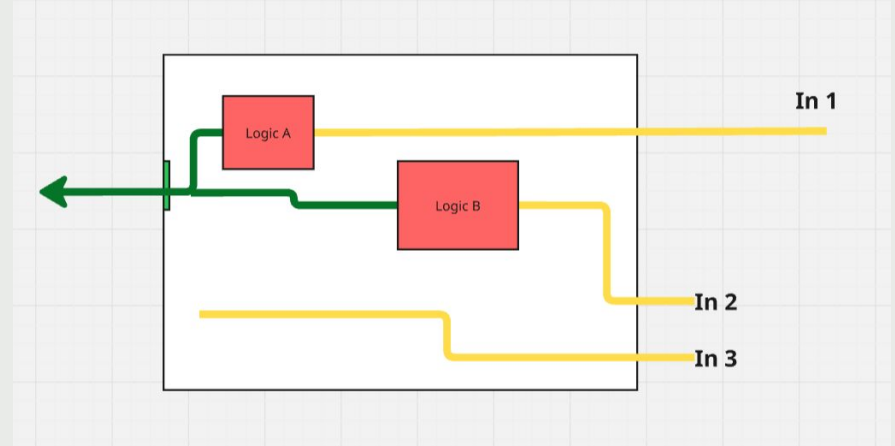
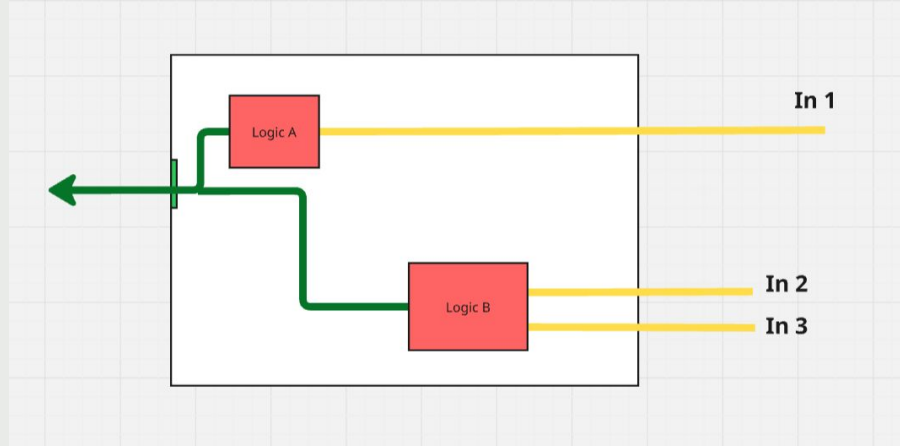
Configurations

Configuration Name	RECONFIG_LEDS	RECONFIG_PMOD
config_LightControl	LED_LeftWalk	PMOD_LightControl
config_MotorControl	LED_rightWalk	PMOD_MotorCNTRL
config_noControl	LED_LeftWalk	PMOD_LeftRight

Configuration Runs

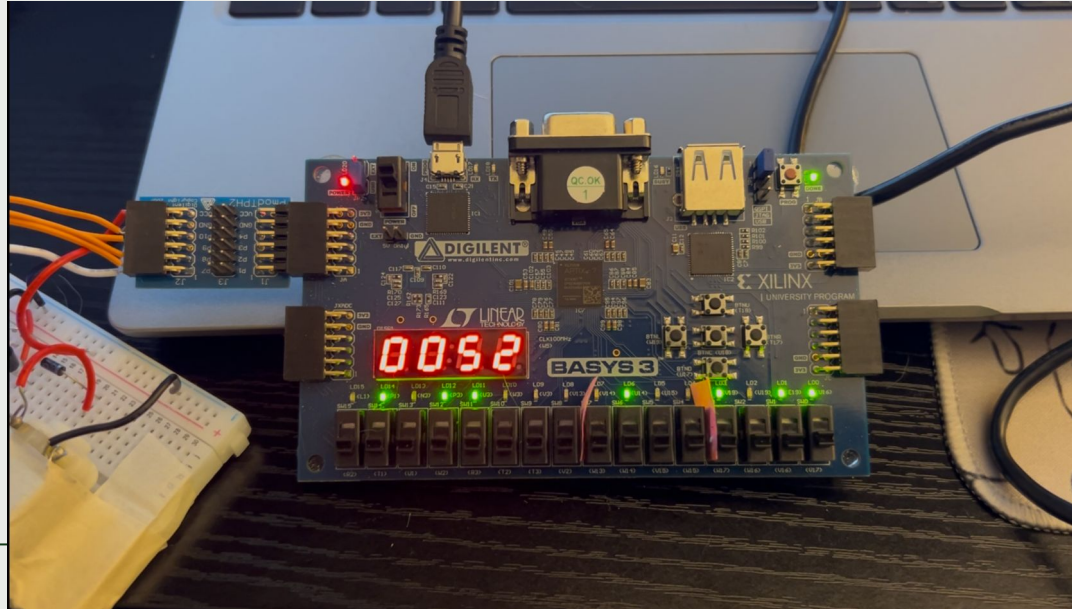
Name	Configuration	Parent	Constraints	Run
impl_1	config_noControl	synth_1	constrs_1 (active)	V
impl_NOcnrl	config_noControl	synth_1	constrs_1 (active)	V
impl_MOTOR_CNRL	config_MotorControl	impl_NOcnrl	constrs_1 (active)	V
impl_LED_CNRL	config_LightControl	impl_NOcnrl	constrs_1 (active)	V

If not...



Literally Happened to me

Supposed be a On Board LED Right Walk. Just some randomness. Had to fix it in the DFX, and re-synthesize...



P-Block Drawing Errors

- P-Block Designs that share a Column seems like a no-no
 1. Just move it over to the right or left so that they're not on top of each other (Next Slide)
 2. Add the 'Snap Mode ON' in the constraints file
-

Seems like Row Y99 is the issue

Dynamic Function eXchange (1 error)

Pblock (1 error)

- ❗ [DRC HDPR-25] Reconfigurable Pblocks must not overlap same frame: Reconfigurable Pblocks cannot share a column within a Clock Region. Reconfigurable cell '[RECONFIG_PMOD](#)' in Pblock '[pblock_RECONFIG_PMOD](#)' and reconfigurable cell '[RECONFIG_LEDS](#)' in Pblock '[pblock_RECONFIG_LEDS](#)' violate this rule. The following are 10 of the tiles that are causing overlaps:

CLBLL_L_X2Y99

INT_L_X2Y99

INT_R_X3Y99

CLBLM_R_X3Y99

CLBLL_L_X4Y99

INT_L_X4Y99

INT_R_X5Y99

CLBLM_R_X5Y99

BRAM_INT_INTERFACE_L_X6Y99

INT_L_X6Y99

For further analysis rerun this DRC with the following param:

set_param hd.visual 2

This will create a file named: `hd_visual/pblock_RECONFIG_PMOD_AND_pblock_RECONFIG_LEDS_IllegalOverlapTiles.tcl`, containing a list of the tiles found overlapping. This .tcl file can also be run from the Vivado GUI to view the tiles visually.

- ❗ [Vivado_Tcl 4-78] Error(s) found during DRC. Opt_design not run.

*ChatGPT said X2 through X6 is the issue.



END.

DFX DEMO:

<https://www.youtube.com/watch?v=faAjsjYVUXE>
